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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,422	09/20/2000	Bin Zhao		7422

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,422	ZHAO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 15, 2004 has been entered.

Allowable Subject Matter

2. The indicated allowability of claims 22-23 is withdrawn in view of the newly discovered reference(s) to Buchwalter et al. and Jeng. Rejections based on the newly cited references follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Saul et al. (EP 0 475 646 A2).

Regarding claim 1, Saul et al. teaches a method for fabricating a damascene interconnect structure having one or more air trenches (16) and a plurality of spaced-apart metal lines (4 and 5) comprising:

(a) fabricating the damascene structure to a via level through a processing step prior to forming contact vias (see figs. 2 and 3), wherein step (a) comprises:

depositing a first dielectric layer (3);

depositing a first capping layer (6) over the first dielectric layer; and

depositing a second capping layer (9) directly on the first capping layer;

(b) etching one or more air trenches (16) into the damascene structure so that the air trenches (16) are positioned between selected metal lines (4 and 5) (col. 4, lines 39-42), wherein the second capping layer (9) is situated over the selected metal lines (4 and 5) (see Figs. 2 and 3); and

(c) depositing a sealing layer over the damascene structure having air trenches to seal the air trenches (see col. 4, lines 13-20).

5. Claims 1-8 and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Buchwalter et al. (US Pat. No. 6,184,121 B1).

Regarding claims 1-2, 29, Buchwalter et al. teaches a method for fabricating a damascene interconnect structure having one or more air trenches and a plurality of spaced-apart metal lines comprising:

(a) fabricating the damascene structure to a via level through a processing step prior to forming contact vias (90) (see fig. 4A), wherein step (a) comprises:

depositing a first dielectric layer (20) (see fig. 2C);

depositing a first capping layer (30) over the first dielectric layer (see fig. 2C);

depositing a second capping layer (20) over the first capping layer (30) (see fig. 2D), wherein the second capping layer is situated over the selected metal lines (70) shown in fig. 2C);

depositing a second dielectric layer (30) over the second capping layer (20) (see fig. 2D); and

depositing a third capping layer (20) over the second dielectric layer (30) (Not shown)[1];

(b) etching one or more air trenches into the damascene structure so that the air trenches are positioned between selected metal lines (70) (see fig. 4A and col. 6, lines 53-61);

(c) depositing a sealing layer (120) over the damascene structure having air trenches to seal the air trenches (110) (see fig. 4C); and

[1] Please note that the sequence of steps for forming the structure shown in figure 2C can be repeated several times until the necessary number of wiring layers are built (col. 2, lines 20-22). For example, the steps can be repeated three times so that a multilevel structure comprising three pairs of insulating layers 20 and 30 is formed.

(d) depositing a polish or etch stop layer (130) over the sealing layer (see fig. 4C).

Regarding claims 3 and 30, Buchwalter et al. further teaches etching an air trench in the first and second dielectric layers, and the first, second and third capping layers (see fig. 4A).

Regarding claims 4-8, Buchwalter et al. further teaches:

forming a via in the sealing layer (120) and the damascene structure (100) (consider the opening formed in layers 100 and 120 as shown in figure 4D);

forming a trench over the sealing layer (consider the opening formed in the layer 130 as shown in figure 4D); and

forming a conductive layer (90), which forms a conductive layer (upper portion of the conductive layer) in the opening formed in layer (130) and a metal plug (bottom portion of the conductive layer) in the opening formed in layers (100) and (120) (see fig. 4D).

6. Claims 1 and 4-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (US Pat. No. 6,159,840).

Regarding claim 1, Wang teaches a method of forming a semiconductor device comprising the steps of:

a) fabricating the damascene structure (see the structure shown in figure 2A) to a via level (202) (see fig. 2A) through a processing step prior to forming contact vias (220a) (see fig. 2F), wherein step (a) comprises:

depositing a first dielectric layer (204) (see fig. 2A),

depositing a first capping layer (206) over the first dielectric layer (204) (see fig. 2A); and

depositing a second capping layer (208) directly on the first capping layer (see fig. 2A);

b) etching one or more air trenches (212b) into the damascene structure so that the air trenches are positioned between selected metal lines (202) (see fig. 2B), wherein the second capping layer (208) is situated over the selected metal lines (202) (see Fig. 2B); and

c) depositing a sealing layer (214) over the damascene structure having air trenches (212b) to seal the air trenches (213) (see fig. 2C).

Regarding claim 4, Wang further teaches the steps of: forming a via (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the sealing layer (214) (see fig. 2E); forming a conductive layer (220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

Regarding claim 5, Wang further teaches the steps of: depositing an etch stop layer (216) over the sealing layer (214) (see fig. 2D); forming a via (212a) in the etch stop layer, the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the etch stop layer (214) (see fig. 2E); forming a conductive layer (220) in the trench (218) (see fig. 2F); and forming a metal plug (220a) in the via (212a) (see fig. 2F).

Regarding claims 6-8, Wang further teaches the steps of: forming a via (212a) in the sealing layer (214) and the damascene structure (see fig. 2E); forming a trench (218) over the sealing layer (214) (see fig. 2E); and forming a conductive layer (220) in the trench (218) (see fig. 2F).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchwalter et al. (US Pat. No. 6,184,121 B1) in view of Jeng (US Pat. No. 5,708,303).

Regarding claim 21, Buchwalter et al. teaches a method for fabricating a damascene interconnect structure having one or more air trenches and a plurality of spaced-apart metal lines comprising:

(a) fabricating the damascene structure to a via level through a processing step prior to forming contact vias (90) (see fig. 4A),

(b) etching one or more air trenches into the damascene structure so that the air trenches are positioned between selected metal lines (70) (see fig. 4A and col. 6, lines 53-61);

(c) depositing a sealing layer (120) over the damascene structure having air trenches to seal the air trenches (110) (see fig. 4C); and

(d) depositing a polish stop layer (130) over the sealing layer (see fig. 4C).

However, Buchwalter et al. is silent with respect to depositing an etch stop layer directly on the polish stop layer. Jeng teaches that it is well known in the art to deposit an etch stop layer (50) directly on the polish stop layer (52) (see fig. 4).

Buchwalter et al. and Jeng are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to deposit an etch stop layer directly on the polish stop layer. The motivation for doing so, as is taught by Jeng, is controlling trench depth (col. 3, lines 34-38). Therefore, it would have been obvious to combine Jeng with Buchwalter et al. to obtain the invention of claims 21-28.

Regarding claim 22, Buchwalter et al. further teaches that the step (a) comprises:

depositing a first dielectric layer (20) (see fig. 2C);

depositing a first capping layer (30) over the first dielectric layer (see fig. 2C);

depositing a second capping layer (20) over the first capping layer (30) (see fig. 2D), wherein the second capping layer is situated over the selected metal lines (70) shown in fig. 2C);

depositing a second dielectric layer (30) over the second capping layer (20) (see fig. 2D); and

depositing a third capping layer (20) over the second dielectric layer (30) (Not shown)[2].

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[2] Please note that the sequence of steps for forming the structure shown in figure 2C can be repeated several times until the necessary number of wiring layers are built (col. 2, lines 20-22). For example, the steps can be repeated three times so that a multilevel structure comprising three pairs of insulating layers 20 and 30 is formed.

Regarding claim 23, Buchwalter et al. further teaches etching an air trench in the first and second dielectric layers, and the first, second and third capping layers (see fig. 4A).

Regarding claims 24-28, Buchwalter et al. further teaches:

forming a via in the sealing layer (120) and the damascene structure (100) (consider the opening formed in layers 100 and 120 as shown in figure 4D);

forming a trench over the sealing layer (consider the opening formed in the layer 130 as shown in figure 4D); and

forming a conductive layer (90), which forms a conductive layer (upper portion of the conductive layer) in the opening formed in layer (130) and a metal plug (bottom portion of the conductive layer) in the opening formed in layers (100) and (120) (see fig. 4D).

Response to Arguments

8. Applicant's arguments with respect to claims 1-8 and 21-30 have been considered but are moot in view of the new grounds of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
11/14/04

GEORGE ECKERT
PRIMARY EXAMINER